L18: Entry 7 of 26 File: USPT Apr 1, 1997

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TITLE: Message passing system for distributed shared memory multiprocessor system and message passing method using the same

Abstract Text (1):
In a multiprocessor system, each processor module comprises a processor, a distributed shared memory, a distributed memory coupler for controlling copying between distributed shared memories and a distributed memory protector for protecting said distributed shared memory against illegal access. The distributed shared memories are assigned global addresses common to all the processor modules, and the distributed shared memory of each processor module has its addresses shared with the distributed shared memory of each processor module which is the destinatiion of data transfer. Message buffers and message control areas on the distributed shared memory are divided into areas specified by a combination of sending and receiving processor modules. A processing request area on the distributed shared memory is divided corresponding to each receiving processor module and arranged accordingly. The processing request area on the receiver's side distributed shared memory has a FIFO structure. The sender's side distributed memory coupler stores identifying information of the destination processor module between the processor module communication and, upon occurrence of a write into the distributed shared memory, sends a write address and write data to the destination processor module. The receiver's side distributed memory coupler copies the received write data into the distributed shared memory of the processor module to which the distributed shared memory coupler belongs, by receiving write address and write data from the sender's side distributed memory coupler.

Detailed Description Text (38):
Next, a description will be given of constituents in the distributed memory coupler 22. A bus signal decoder 31 decodes a signal on the signal line of the processor bus 30 and, upon occurrence of write access to the distributed shared memory 21, provides a "1" onto a signal line 32 to activate a transfer control part 33. The transfer control part 33 exerts control over the distributed memory coupler 22 and feeds various control signals (not shown) to internal logics. A module ID management part 34 prestore the destination processor module ID(PM.sub.-- ID) that is needed when write data to the distributed shared memory 21 is transferred to and from the processor modules. The module ID management part 34 will be described later in more detail with reference to FIG. 6. A packet send register 35 stores a distributed shared memory address and write data to be transferred to another processor module or interrupt information to another processor module. A packet send buffer 36 provides a feature which receives data from the packet send register 35 and temporarily holds it until it is transferred to another processor module. A packet receive buffer 37 provides a feature which receives data transferred from another processor module and temporarily holds it until it is delivered to a packet receive register 38. A packet decoder 39 decodes data in the packet receive register 38 and, if the decoded result is a request for write into an address location in the distributed shared memory 21, then the packet decoder 39 sends a request via a signal line 40 to the transfer control part 33 for the write into the distributed shared memory 21. If the decoded result is an interrupt from another processor module, then the packet decoder 39 sends an interrupt processing request via a signal line 41 to an interrupt control part 42. The interrupt control part 42 responds to the request to send an interrupt request to the processor 19 via a signal line 43.

Detailed Description Text (54):
In the distributed memory coupler 22 at the receiving processor module, the packet receiving buffer 37 receives the data transferred from the sending processor module and hands it over to the packet receiving register 38. The packet receiving register 38 decodes the received data and writes it in the specified address location in the distributed shared memory 21. In this way, data is copied from the sender's distributed shared memory to the receiver's distributed shared memory. Incidentally, write access to the sender's distributed shared memory is completed before copy access to the receiver's distributed shared memory is completed.

Detailed Description Text (143):
First, when the processor (19-1) of the sending processor module PM#1 (18-1) executes an instruction to write to the MB management map entry (XM12-1), its address and the write data are provided onto the processor bus 30-1 in FIG. 5. In the sender's distributed memory coupler 22-1, the bus signal decoder 31-1 detects write access to the sender's distributed shared memory 21-1 and activates the transfer control part 33-1 via the signal line 32-1. The transfer control part 33-1 takes in the address of the MB management map entry (XM12-1) and the write data and feeds the page address of the MB management map entry (XM12-1) to the module ID management part 34-1. Since there is prestored in the CAM command register 67-1 (FIG. 6) a command that instructs "COMPARISON WITH KEY REGISTER 65-1," the entries of the key register 65-1 and the CAM cell part 61-1 are compared when the page address of the MB control map entry (XM12-1) is loaded into the key register (65-1). Each entry of the CAM cell part 61-1 contains the page address SPA shared by other processor modules. In this embodiment, the pair of the page address PA-M of the MB management map entry XM12-1 shared with the receiving processor module (18-2) and the identification number of the receiving processor module (18-2), i.e. PM.sub.--ID are stored in the CAM cell part (61-1) and the data memory part (62-12), respectively. Consequently, a match is detected between the key register 65-1 and the CAM cell part 61-1, and the identification number of the corresponding receiving processor module (18-2) is taken out from the data memory part 62-1. This identification number is transferred to the packet sending register 35-1 (FIG. 5). As shown in FIG. 7, "0" is set in the attribute identification field in the packet sending register 35-1 to indicate that the packet is the distributed shared memory access type and the identification number of the processor module (18-2 ) is set in the destination PM.sub.-- ID field 81 which has been taken out from the module ID management part 34-1. Furthermore, the address (the address of the MB management map entry XM12-1) and the write data ("OCCUPIED") on the processor bus 30-1 are set in the distributed shared memory address field 82 and the write data field 83, respectively, and a signal specified by the processor bus 30-1 (in concrete terms, the write width) is set in the write width field 84. The sending packet is thus assembled. When supplied with this packet, the packet sending buffer 36-1 (FIG. 5) provides it onto the processor interconnect 25. Based on the destination PM.sub.--ID field 81 of the packet, the processor interconnect 25 routes the packet to the packet receiving buffer 37-2 of the receiving processor module PM#2 (18-2).

Detailed Description Text (144):
In the receiving processor module PM#2, the data of the packet receiving buffer 37-2 is input into the packet receiving register (38-2) and decoded by the packet decoder 39-2, and when the data is found to be of the distributed shared memory access type, the transfer control part 33-2 is activated. The transfer control part 33-2 sends the distributed shared memory address (the address of the MB management map entry XM12-1), the write data ("OCCUPIED") and the write width information in the packet receiving register 38-2 to the distributed shared memory 21-2 via the processor bus 30-2. As the result of this, the same value of the write data for the MB management map entry XM12-1 is written into the receiver's distributed shared memory 21-2 at the same address location YM12-1.